

NEUROMORPHIC COMPUTING FOR SPACE

Neuromorphic computing, which draws insights from neuroscience to create chips that function more like the biological brain, aspires to deliver orders of magnitude improvements in energy efficiency, speed of computation and efficiency of learning across a range of edge applications.

AFRL's Neuromorphic Computing Intelligence Systems+ (NICS+)

NICS+ is a 6.2 development and demonstration program, emphasizing integration of advanced neuromorphic technologies into space and airborne experiments for on-system learning. Advance architectures exposing new capabilities for artificial intelligence, machine learning and autonomous solutions for edge computing.

NICS+ Projects and Partners

AFRL's partnership with Intel enables access to the most advanced neuromorphic technologies, such as the Lohi 2 research chip and the Lava open-source software framework for developing neuro-inspired applications. The Spikking Neural Network (SNN) machine learning (ML) applications and related efforts are applying novel techniques using AF data relevant data sets to better understand the limits and metrics. In FY23 and FY24 the novel processing boards will be supporting several experiments for Air and Space.

FalconSAT-X (FSX): Al Neuromorphic-computing Technology Experiment (ANTE)

- 1st Neuromorphic AI/ML Intelligent Computing in Space
- Pathfinder for future Space Force on on-orbit Multi-INT data processing at the edge

Neuromorphic Computing for Space

There are several benefits to neuromorphic computing that are particularly advantageous for use in the space domain.

- Ultra-low power (~100 mW) could enable 24/7 operations for constrained small satellites and rovers
- Inherently parallel architecture supports redundancy and information-theoretic means for detecting and masking or correcting errors
- Chips like Loihi incorporate error-correcting memory modules that reduce uncorrectable bitflips
- Probabilistic foundation of neural nets is more fault-resistant than deterministic processing and can be further enhanced with training and on-chip learning

